WHAT IS CLAIMED IS:

1. A control system for a counter for supplying addresses to a device having a first contiguous address region and a second address region that corresponds thereto and that has a non-contiguous region portion, the address-counter control system comprising:

a counter circuit having address counters, the number of address counters corresponding to the first address region, the address counters comprising a first series of address counters which corresponds to the non-contiguous region portion and second and third series of address counters which correspond to respective contiguous region portions and which are located at two opposite ends of the first series of address counters;

path switches that are provided at connection paths between the second and the third series of address counters, wherein the path switches disconnect the first series of address counters and directly connect the second and third series of address counters or disconnect the direct connection between the second and third series of address counters and connect the first series of address counters to and between the second and the third series of address counters; and

a control circuit, wherein, for forming the first address region, the control circuit controls the path switches to disconnect the direct connection between the second and the third series of address counters and connect the first series of address counters to and between the second and the third series of address counters, so that the non-contiguous region is placed in the first address region, and sequentially causes counting of the first, second, and third series of address counters, and wherein, for putting the second address region into a contiguous state, the control circuit controls the path switches to disconnect the first

series of address counters and directly connect the second and third series of address counters and sequentially causes counting of the second and third series of address counters.

2. A control system according to claim 1, wherein:

when all address counting for the first address region is completed in response to an output from an address counter for a final address in the first address region, the control circuit drives the path switches to start address counting for the second address region, and when all address counting is completed in response to an output from an address counter for a final address in the second address region, the control circuit generates an end signal indicating that all address counting for the first and second address regions is completed.

3. A control system for a refresh counter for a memory device that requires refreshing and that includes a normal address region having "nth power of 2" contiguous addresses and a parity address region having a non-contiguous address region portion with non-contiguous addresses, the number of non-contiguous addresses being different from "nth power of 2", the address-counter control system comprising:

a counter circuit having address counters, the number of address counters corresponding to the normal address region, the address counters comprising a first series of address counters which corresponds to the non-contiguous address region portion and second and third series of address counters which correspond to respective contiguous region portions and which are located at two opposite ends of the first series of address counters;

path switches that are provided at connection paths between the

second and the third series of address counters, wherein the path switches disconnect the first series of address counters and directly connect the second and third series of address counters or disconnect the direct connection between the second and third series of address counters and connect the first series of address counters to and between the second and the third series of address counters; and

a control circuit, wherein, for forming the normal address region, the control circuit controls the path switches to disconnect the direct connection between the second and the third series of address counters and connect the first series of address counters to and between the second and the third series of address counters, so that the non-contiguous address region portion is placed in the normal address region, and sequentially causes counting of the first, second, and third series of address counters, and wherein, for putting the parity address region into a contiguous state, the control circuit controls the path switches to disconnect the first series of address counters and directly connect the second and third series of address counters and sequentially causes counting of the second and third series of address counters.

4. A control system according to claim 3, wherein:

during a refresh operation of the memory device, when all address counting for the normal address region, starting from a first address counter corresponding to the normal address region, is completed in response to an output from an address counter for a final address in the normal address region, the control circuit drives the path switches to start address counting for the parity address region, and when all address counting is completed in response to an output from an address counter for a final address in the parity address region, the control circuit generates a refresh end signal indicating that all address

counting for both of the normal and parity regions is completed.

5. A control system according to claim 3, wherein:

the control circuit retains a counter value of one of the address counters, and during a refresh operation of the memory device, for the normal region, the control circuit causes counting of an address counter following the address counter whose counter value is retained, and, in response to an address counter output that matches the retained counter value, the control circuit drives the path switches to start address counting for the parity address region, wherein, when all address counting for the parity address region is completed and the retained counter value is reached, the control circuit generates a refresh end signal indicating that all address counting for both of the normal and parity regions is completed.

6. A control system according to claim 5, wherein:

when an address corresponding to the retained address counter value is in the non-contiguous address region portion, a count value of a first address following the non-contiguous address region portion in the parity address region is substituted for the retained counter value.